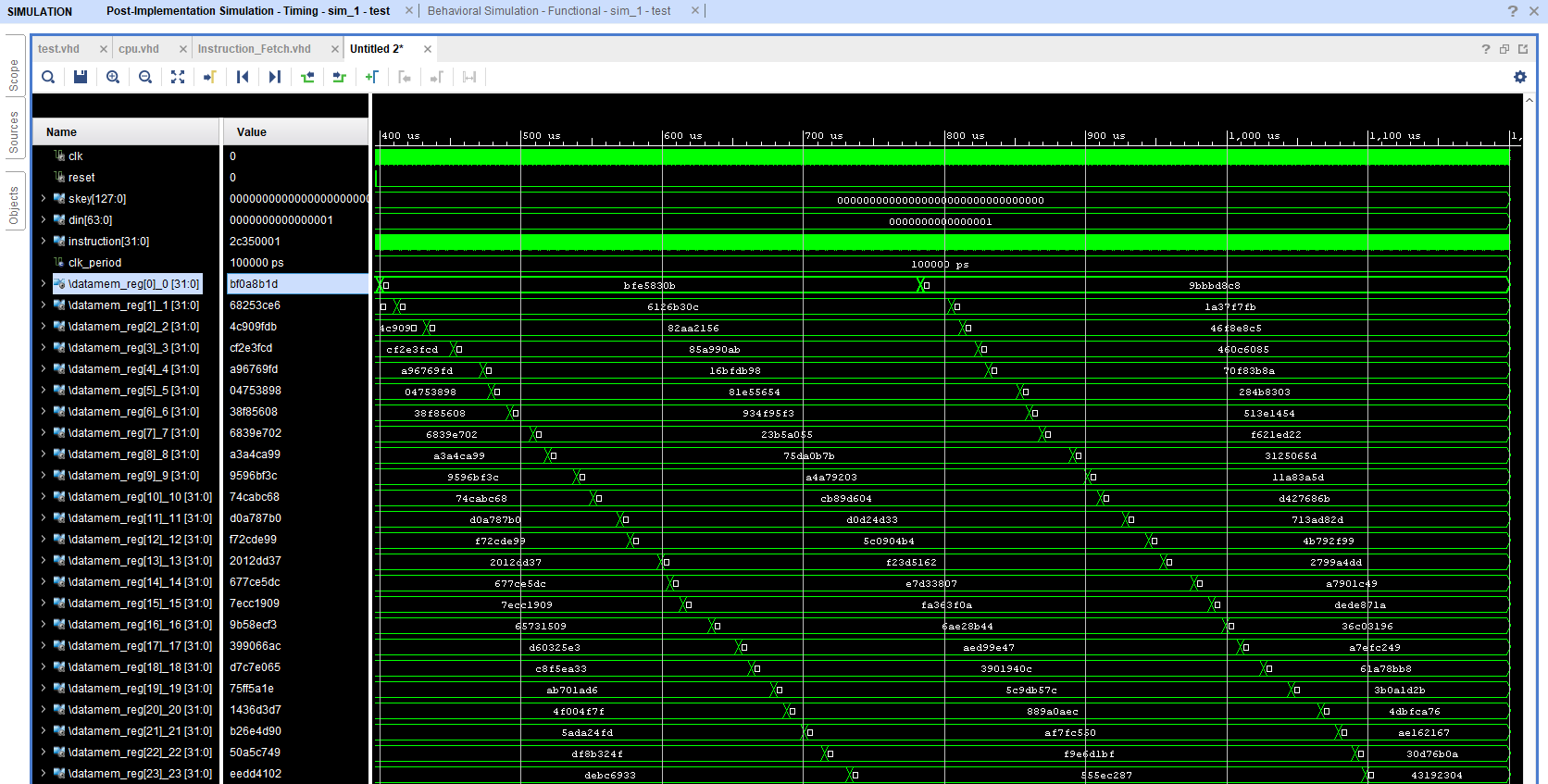
In our assembly code, the order of the excution is do key expansion, then encoding, then decoding.

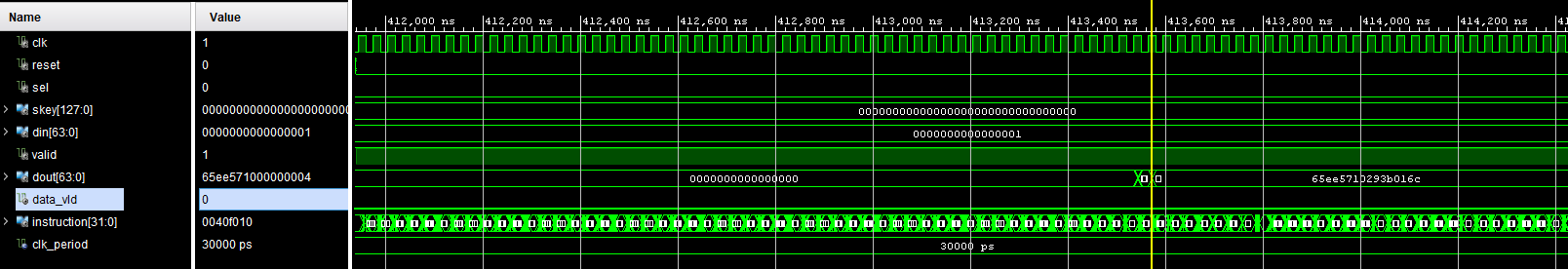
In our timing simulation, we first set the selection signal to 0 and get the value of encoding result, then we set the selection signal to 1 and wait for a while to get the result of decoding.

**Key expansion part**

We save the Skey to Data memory[25 downto 0], as we can see the data memory is filled and updated during the simulation.

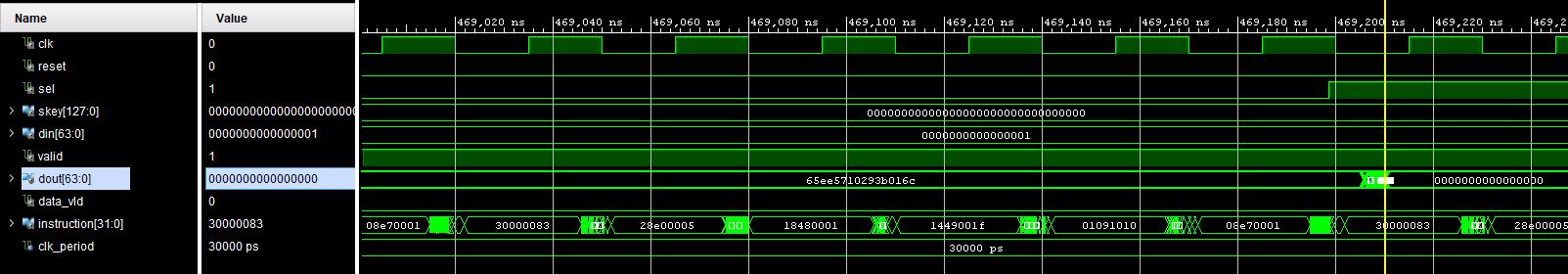


**Encoding part**



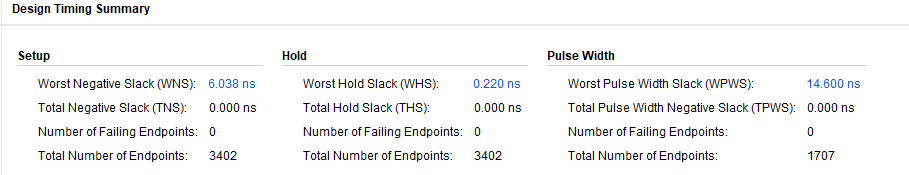
**Decoding part**

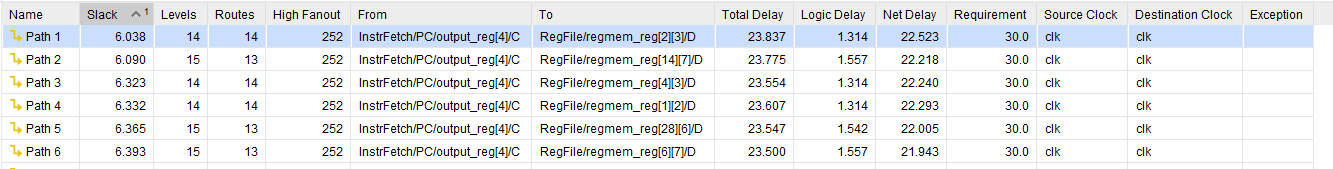
As we can see, after we got the value of encoding result, we first set the selection signal to 1, and now dout changed to 0, since the decoding result is not generated yes, and after a while, we got the correct decoding value in result and the instruction also stopped at HALT.



Critical Path Delay:

We set the timing constrain to 30ns.

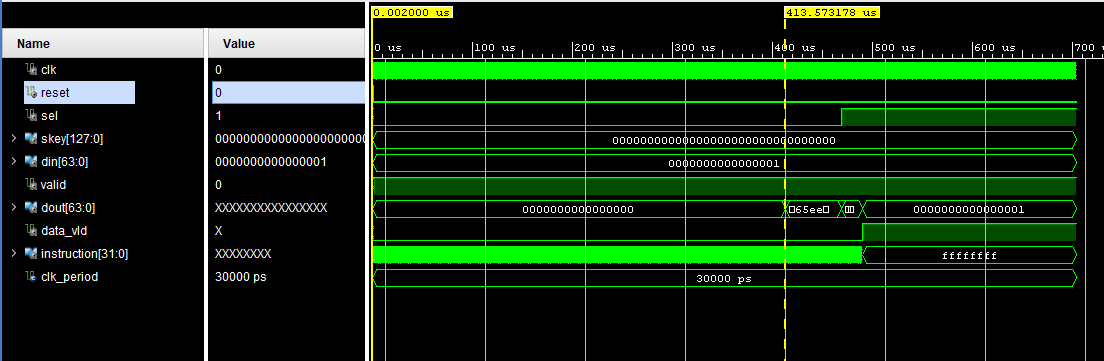




Critical path delay: 23.837ns

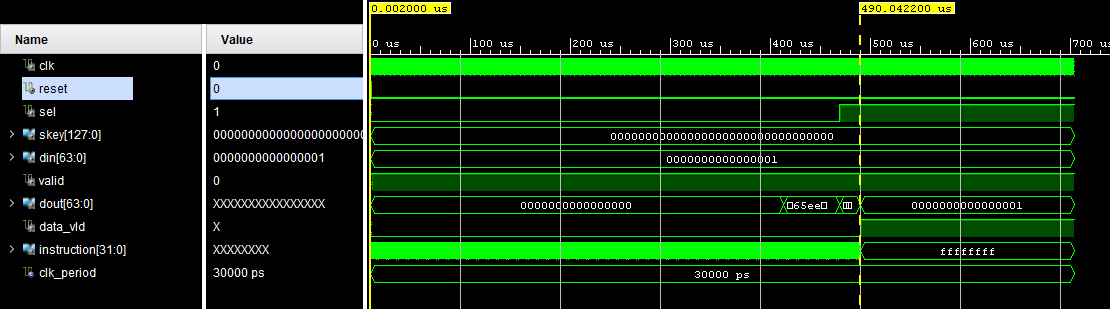
Max Frequency: 41.96MHz

Latency of encode



Latency = = 10338 clock cycles.

Latency of decode



Latency = = 12250 clock cycles.